REMARKS/ARGUMENTS

In the Office Action, the Examiner noted that claims 1-9, 15-16, 32-40, and 46 are pending in the application. The Examiner additionally stated that claims 1, 3, 4, 9, and 32 are rejected and that claims 2, 5-8, 15, 16, 33-40, and 46 are objected to. By this amendment, claims 2 and 33 are cancelled and claims 1, 32, 34, and 46 are amended. Hence, claims 1, 3-9, 15-16, 32, 34-40, and 46 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

In the Specification

Applicant has amended the specification to secure a substantial correspondence between the claims amended herein and the remainder of the specification. No new matter is presented.

In the Claims

Rejections Under 35 U.S.C. §112

The Examiner rejected claim 46 under 35 U.S.C. 112, second paragraph, as being indefinite for facility to particularly point out and distinctly claim the subject matter which Applicant regards as the invention, noting that claim 46 recites the limitation "the second one of the plurality of part-page ownership bits" in lines 2-3, and that there is insufficient antecedent basis for this limitation in the claim.

In response, Applicant has amended claim 46 to depend rather from claim 35, thus providing the antecedent basis. Accordingly, Applicant requests that the rejection of claim 46 be withdrawn.

Allowable Subject Matter

The Examiner objected to claims 2, 5, 33, and 36 as being dependent upon a rejected base claim, but indicated that these claims would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The Examiner also noted that claims 6-8, 15-16, 34-35, 37-40, and 46 would be allowable as the further limit the objected claims 5, 33, and 36.

Applicant appreciates the Examiner's consideration and indications of allowability of these claims. By this amendment, the allowable limitations of claim 2 have been incorporated into the language of claim 1 and the allowable limitations of claim 33 have been incorporated into the language of claim 32. Claims 2 and 33 have been cancelled and those claims depending from claims 2 and 33 have been amended to now depend from claims 1 and 32, as appropriate.

Rejections Under 35 U.S.C. §103

The Examiner rejected claims 1, 3-4, 9, and 32 under 35 U.S.C. 103(a) as being unpatentable over Kyker et al., U.S. Patent No. 6,594,734 (hereinafter, "Kyker").

As per claim 1, the Examiner stated that Kyker teaches an apparatus in a pipeline microprocessor (i.e. 301A in Fig. 4A), for ensuring coherency of instructions within stages of the pipeline microprocessor, the apparatus comprising: instruction cache management logic (i.e. 41 5 in Fig. 4A), configured to receive an address corresponding to a next instruction to be fetched (i.e. the physical address received by the ITLB), and configured to detect that a part of a memory page corresponding to said next instruction cannot be freely accessed without checking for coherency of the instructions within said part of said memory page (i.e. the physical addresses stored in ITLB) and, upon detection, configured to provide said address; and synchronization logic, configured to receive said address from said instruction cache management logic, and configured to direct data cache management logic to check for coherency of the instructions within said part of said memory page, and, if the instructions are not coherent within said part of said memory page, said synchronization logic is configured to direct the pipeline microprocessor to stall a fetch of said next instruction until the stages of the pipeline microprocessor have executed all preceding instructions (e.g. see the abstract, claim 17 and Fig. 4A). The Examiner noted also that Kyker further discloses that when a snoop is triggered, the physical address of the store into memory is provided to the snoop port and the ITLB performs a comparison with all the physical page addresses located within the ITLB 412 to determine whether a store into memory has addressed a page which may be stored in the instruction cache 414A. The Examiner stated that if a match is found, a

store occurred into memory within a page of instructions that may be stored within an instruction cache and the cache and the instruction pipeline may be incoherent with memory (e.g. see Col. 7, lines 6-15), stating, in other words, Kyker does teach that the instruction cache management logic evaluates an instruction translation lookaside buffer (ITLB) entry corresponding to the address of the next instruction to detect that said part cannot be freely accessed, as claimed. The Examiner conceded that although Kyker does not specifically disclose that the data cache management logic evaluates a DTLB entry corresponding to the address to detect that the instructions are not coherent within said part of the memory page, Kyker does teach, in Col. 7, lines 6-15, about evaluating ITLB entry corresponding to the address to detect that the instruction is not coherent within the part of the memory page, and that Kyker also discloses that "[Tlhe present invention has been described herein with reference to instructions in an instruction translation lookaside buffer (ITLB) and an instruction cache, but it is equally applicable for cache coherency between memory and a cache storing data where a translation lookaside buffer is used" (e.g. see Col. 14, lines 16+).

The Examiner therefore concluded that it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to also evaluate a DTLB entry corresponding to the address of the next instruction to detect that the instructions are not coherent within said part of the memory page and, in doing so, the data coherency within the part of the memory page can be detected.

As per claim 32, the Examiner opined that Kyker teaches a method in a pipeline microprocessor (i.e., 301 in Fig. 4A), for ensuring coherency of instructions within stages of the pipeline microprocessor, the apparatus comprising: within instruction cache (i.e. 414A in Fig. 4A), detecting that a part of a memory page corresponding to a next instruction to be fetched cannot be freely accessed without checking for coherency of the instructions within the part of the memory page; directing logic within a data cache to check for coherency of the instructions within the part of the memory page; and if the instructions are not coherent, stalling a fetch of the next instruction from the instruction cache until the stages of the pipeline microprocessor have executed all preceding instructions (e.g., see the abstract, claim 17 and Fig. 4A). The Examiner further stated

that Kyker discloses that when a snoop is triggered, the physical address of the store into memory is provided to the snoop port and the ITLB performs a comparison with all the physical page addresses located within the ITLB 412 to determine whether a store into memory has addressed a page which may be stored in the instruction cache 414A, and that if a match is found, a store occurred into memory within a page of instructions that may be stored within an instruction cache and the cache and the instruction pipeline may be incoherent with memory (e.g., see Col. 7, lines 6-1 5). The Examiner added that Kyker does teach that the instruction cache management logic evaluates an instruction translation lookaside buffer (ITLB) entry corresponding to the address of the next instruction to detect that said part cannot be freely accessed, as claimed, but granted that although Kyker does not specifically disclose that the data cache management logic evaluates a DTLB entry corresponding to the address to detect that the instructions are not coherent within said part of the memory page, Kyker does teach, in Col. 7, lines 6-15, about evaluating ITLB entry corresponding to the address to detect that the instruction is not coherent within the part of the memory page. The Examiner additionally noted that Kyker also discloses that "[Tlhe present invention has been described herein with reference to instructions in an instruction translation lookaside buffer (ITLB) and an instruction cache, but it is equally applicable for cache coherency between memory and a cache storing data where a translation lookaside buffer is used" (e.g. see Col. 14, lines 16+). The Examiner therefore concluded that it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to also evaluate a DTLB entry corresponding to the address of the next instruction to detect that the instructions are not coherent within said part of the memory page, and in doing so, the data coherency within the part of the memory page can be detected.

By this communication, claims 1 and 32 are amended to include subject matter which is noted above as being allowable over the prior art of record. Consequently, it is requested that the rejections of claims 1 and 32 be withdrawn.

For the purpose of expediting the patent application process in a manner consistent with the PTO's Patent business Goals (PBG), 65 Fed. Reg. 54603 (September 8, 2000), Applicant has elected to amend claims 1 and 32 to incorporate the subject matter which

has been deemed above as being allowable over the prior art of record, that is, the limitations of claims 2 and 33. Claims 2 and 32 are hereby cancelled. However, Applicant respectfully traverses the rejections of claims 1 and 32 and hereby provides notice of intent to pursue these claims in a continuation application.

With respect to claims 3-4 and 9, these claims depend from claim 1 and add further limitations over that subject matter which has been noted above as being allowable over the prior art of record. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejections of claims 3-4 and 9.

CONCLUSIONS

Applicant believes this to be a complete response to all of the issues raised in the instant office action and further submits, in view of the amendments and arguments advanced above, that claims 1, 3-9, 15-16, 32, 34-40, and 46 are in condition for allowance. Reconsideration of the rejections is requested, and allowance of the claims is solicited.

Applicant also notes that any amendments made by way of this response, and the observations contained herein, are made solely for the purpose of expediting the patent application process in a manner consistent with the PTO's Patent business Goals (PBG), 65 Fed. Reg. 54603 (September 8, 2000), and are furthermore made without prejudice to Applicant under this or any other jurisdictions. It is moreover asserted that insofar as any subject matter might otherwise be regarded as having been abandoned or effectively disclaimed by virtue of amendments made herein and/or incorporated in attachments submitted with this response, Applicants wishes to reserve the right and hereby provides notice of intent to restore such subject matter and/or file a continuation application in respect thereof.

Applicant earnestly requests that the Examiner contact the undersigned practitioner by telephone if the Examiner has any questions or suggestions concerning this amendment, the application, or allowance of any claims thereof.

I hereby certify under 37 CFR 1.8 that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on the date of signature shown below.

Respectfully submitted,
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04/06/2007

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